

1st Workshop on Advanced Real-time Processor Architectures ARPA'2013

**Berlin, January 22, 2013
in conjunction with the 8th HiPEAC Conference**

ARPA focuses on advanced time-predictable processor and network-on-chip architectures, memory hierarchies, system software, and analysis techniques for single-, multi-, and many-core systems with emphasis on hard real-time systems.

In general, processors used in hard real-time systems are comparatively simple processors with respect to those used in high-performance systems. This is because hard real-time systems need to be analyzable in terms of timing. However, there is an increasing requirement to provide high-performance in hard-real time systems. The complex performance-improving hardware and software features, well-known from high performance processors are not analyzable at all. Consequently, those features cannot be directly applied to hard real-time systems. ARPA targets this issue by presenting the latest achievements of three STREP FP7 projects: parMERASA, T-CREST and PROARTIS. In particular the workshop will cover hardware designs, dedicated system software, adapted application software, as well as novel analysis techniques for these types of systems.

ARPA joins experts from the three EC funded projects parMERASA, T-CREST, and PROARTIS, which are among the European leading projects in the field of hard real-time systems. The presentations will provide detailed information about the technical issues addressed in the projects together with some preliminary results of ongoing work. Attendees are encouraged to participate and discuss the technical approaches as well as the results.

The workshop is structured into four sessions. The first one introduces all three projects with an overview of each project given by the project coordinators. In the second session, the hardware approaches of the projects are presented while the fourth session shows runtime software support proposed by parMERASA and PROARTIS. The last session concentrates on the tooling support, especially on the worst case execution time analyses of all three projects.

Organization Committee:

Sascha Uhrig, Technical University of Dortmund, Dortmund, Germany
Martin Schoeberl, Technical University of Denmark, Lyngby, Denmark
Francisco J. Cazorla, Barcelona Supercomputing Center, Barcelona, Spain

Please register for the ARPA workshop at

<http://www.hipeac.net/conference/berlin/registration>

The early registration deadline ends on December 21, 2012

Preliminary schedule:

10:00 Introduction of the EU FP7 projects by the project coordinators

Session chairs: Sascha Uhrig, Francisco J. Cazorla

parMERASA – Overview

Theo Ungerer (University of Augsburg)

Overview of the T-CREST Project

Jens Sparsø (Technical University of Denmark)

Introduction to PROARTIS

Francisco J. Cazorla (Barcelona Supercomputing Center)

11:00 Coffee break

11:30 Hardware architectures

Session chair: Christian El-Salloum (TU Vienna)

parMERASA - Hardware Architecture

Eduardo Quiñones (Barcelona Supercomputing Center)

T-CREST - Time-predictable Processor and Network-on-Chip

Jens Sparsø (Technical University of Denmark)

T-CREST - Time-predictable Memory Hierarchy and SDRAM Controller

Kees Goossens (Technical University of Eindhoven)

13:00 Lunch

14:00 PROARTIS Hardware Architectural Solutions

Francisco J. Cazorla (Barcelona Supercomputing Center)

Timing analysis support

Session chair: Jan Reineke (Saarland University)

PROARTIS – WCET Analysis Techniques and Tools

Adriana Gogonel (INRIA)

Ian Broster (Rapita Systems)

parMERASA - WCET Analysis Tools

Haluk Ozaktas (University Paul Sabatier Toulouse)

Ian Broster (Rapita Systems)

T-CREST - Compiler and WCET Analysis Tool Chain

Peter Puschner (Technical University of Vienna)

Gernot Gebhard (AbsInt Angewandte Informatik)

16:00 Coffee break

16:30 System and application software

Session chair: Luis Miguel Pinho (Cister, Porto)

PROARTIS - System Software

Tullio Vardanega (University of Padua)

parMERASA - Parallelized Avionics and Automotive Software

João Fernandes (Honeywell), Sebastian Kehr (Denso Deutschland)

17:30 End of workshop