



T-CREST

Overview of the T-CREST Project

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T-CREST

- T-CREST
 - ◆ Time-predictable Multi-Core Architecture for Embedded Systems
- EC FP7 STREP project
 - ◆ 09/2011 – 09/2014
 - ◆ EC funding 2.65 M EUR
- 4 Universities, 4 industry partners
 - ◆ The Open Group project coordinator
 - ◆ DTU technical lead (Prof. M. Schoeberl)

Partners



Project Goals

- Scope: Hard real-time systems.
- Multi processor platform
 - ◆ Processor nodes
 - ◆ SDRAM memory controller
 - ◆ Network on chip
- Software tools
 - ◆ Compiler
 - ◆ WCET analysis tool
- Benchmark applications

Real-Time Systems

- Systems with timing constraints
 - ◆ In (hard) real-time systems
 - Function has to be correct
 - Function has to deliver result in time
- Timing proof with schedulability analysis
 - ◆ Execution time of tasks need to be known
 - ◆ WCET analysis gives the input

Worst-Case Execution Time

- Measurement of execution time is not safe:
 - ◆ Execution time is data dependent
 - ◆ Did we trigger the worst-case?
- Static WCET Analysis
 - ◆ High-level WCET analysis is mature research
 - ◆ Considers control flow and flow facts (loop bounds)

Static WCET Analysis Issue

- Low-level analysis is the main issue
 - ◆ Modern processors are too complex
 - ◆ Lot of (hidden) state information
 - Key for performance
 - Issue/challenge for WCET analysis
- WCET analysis is about 10 years behind current processors
- Multiprocessors currently not analyzable

New Architectures Needed

- Design a computer architecture for real-time systems
 - ◆ WCET is the main design constraint
 - ◆ Average-case performance not (so) interesting
- Use and develop features that are
 - ◆ WCET analysis driven
 - ◆ Have a low WCET

Time-predictable Computer Architecture

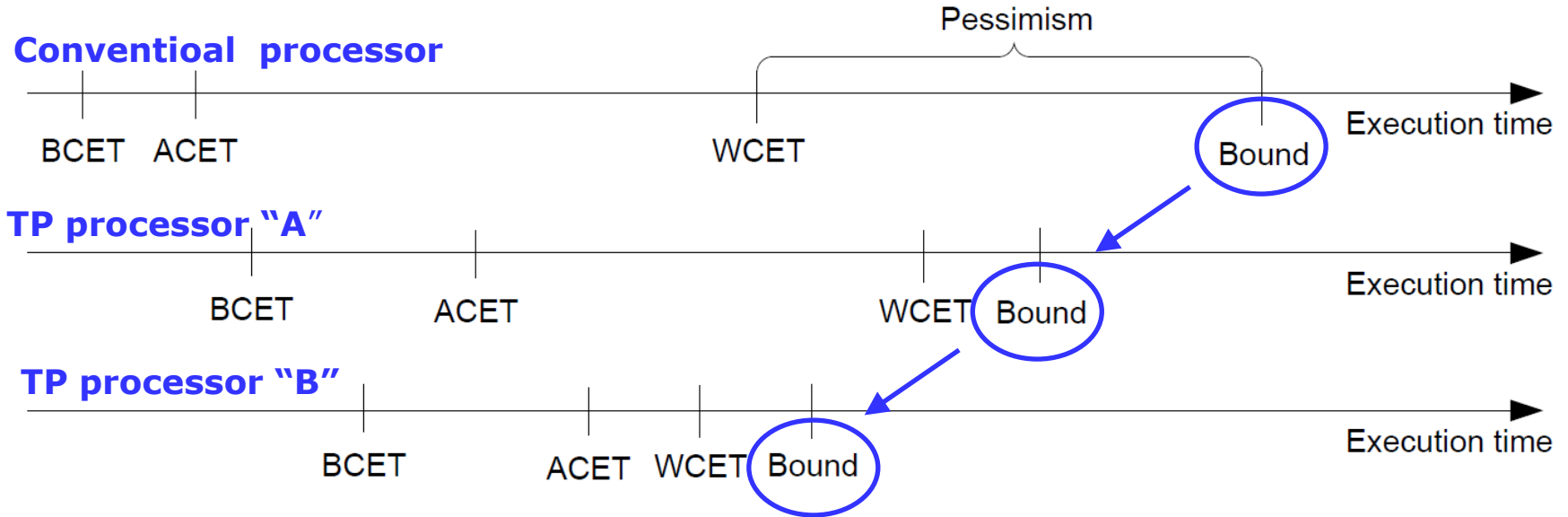
■ Common computer architecture wisdom

*Make the common case fast and
the uncommon case just correct*

■ Time-predictable computer architecture

*Make the worst case fast and
the whole system analyzable*

Our WCET Target Architecture

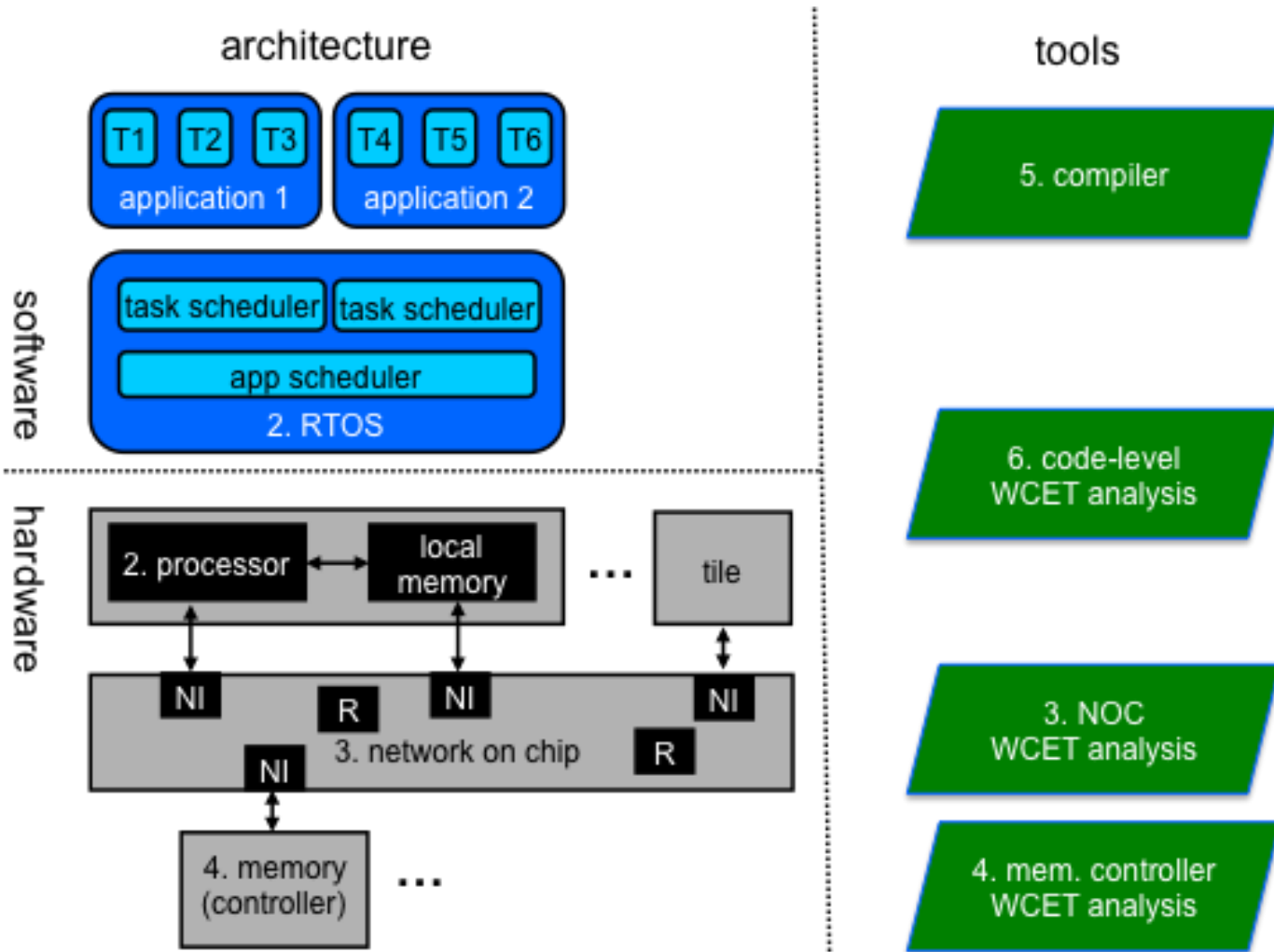


- Trying to catch up with the analysis on the complexity of average case optimized architectures is not an option
- We need a sea change and take a constructive approach. Design processors, memory, and interconnect for real-time systems!

T-CREST Architecture

- Chip-multiprocessor for high performance
 - ◆ Target: 64 core. Prototype in FPGA
- Time-predictable
 - ◆ Processor
 - ◆ Local memory (SPM, \$)
 - ◆ Network-on-Chip (NoC)
 - ◆ SDRAM controller
- Integration in WCET analysis

T-CREST Architecture



Outcome

- A complete CMP platform
 - ◆ Hardware (prototype) in an FPGA
 - ◆ Supporting compiler and WCET analysis tool
- Resulting designs in open source
 - ◆ BSD license
 - ◆ Cooperation welcome
- Up to compiler, i.e., :
 - ◆ No research on operating system
 - ◆ No research on model of computation
 - ◆ No research on automatic parallelization

Work Packages

- WP 1 Requirements Analysis (GMV)
- WP 2 Processor (DTU)
- WP 3 Network on Chip (DTU)
- WP 4 Memory Hierarchy (UoY)
- WP 5 Compiler (TUV)
- WP 6 Code-Level WCET Analysis (AbsInt)
- WP 7 Integration and Evaluation (GMV)
- WP 8 Dissemination (TOG)
- WP 9 Management (TOG)

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- WP 9 Manag

Time-predictable Processor and Network-on-Chip
Jens Sparsø (Technical University of Denmark)

Time-predictable Memory Hierarchy and SDRAM Controller
Kees Goosens (Technical University of Eindhoven)

Compiler and WCET Analysis Tool Chain
Peter Puschner (Technical University of Vienna)
Gernot Gebhard (AbsInt Angewandte Informatik)

T-CREST: More Info

■ T-CREST web site

- ◆ <http://www.t-crest.org/>
- ◆ Most deliverables are public
- ◆ Some first papers

■ Development

- ◆ Most artifacts are open-source
- ◆ Hosted at GitHub
- ◆ <https://github.com/t-crest>