parMERASA

Universität Augsburg University

EC Project parMERASA:
Multi-Core Execution of *parallelised* Hard Real-Time Applications Supporting Analysability

www.parmerasa.eu

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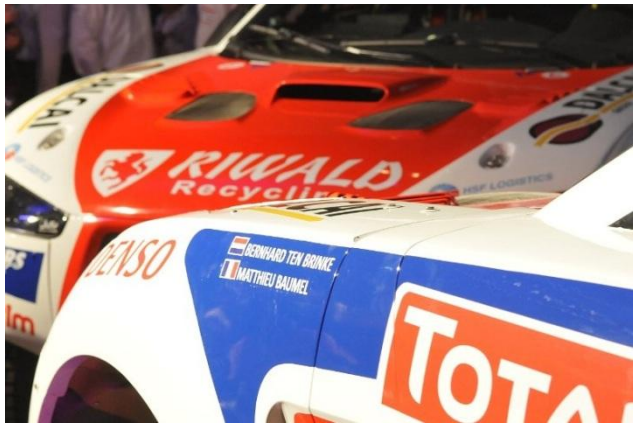
Overview

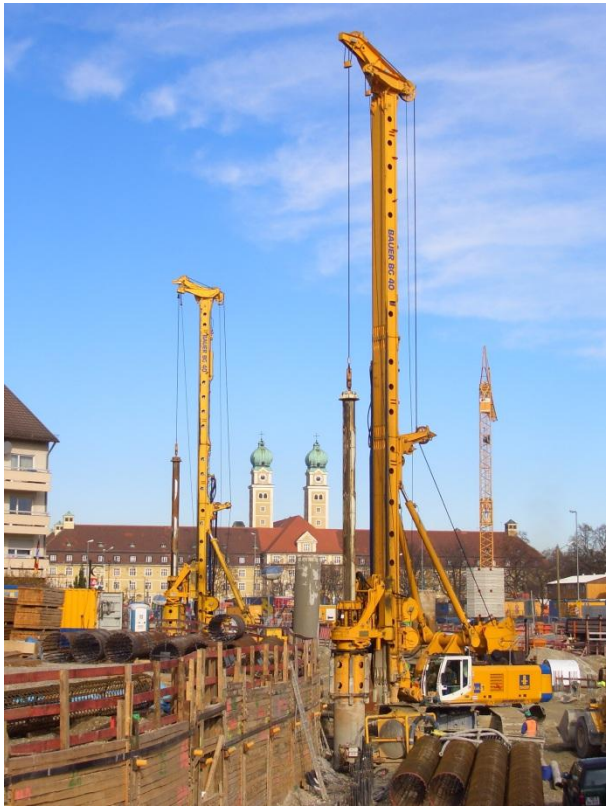
- **Demands on Embedded Processors**
- **Predecessor project MERASA** achievements
- **parMERASA project** overview and targets
- **Conclusions and Vision**

Demands on Embedded Processors

- **Increasing demand** for functionality in current and future real-time embedded systems
- Often demand for **mixed application** execution

Increase of processor performance demanded





Demands on Embedded Processors

- **Time is critical** in embedded systems!

- Safety-related **hard real-time** embedded systems…

  → require that a **deadline must never be missed**,

  → need a **proof of timing requirements by WCET (worst case execution time) analysis**, or

  at least, demonstrate, to an appropriate level of rigour (depending on the criticality of system), that the **implementation meets its timing requirements**.

Motivation

- **Performance is critical** in embedded systems!

- **Multi-core processors** provide a solution for **higher levels of performance** of embedded hard real-time systems.
- However, **timing behaviour of parallel applications is not analysable** with current timing analysis techniques.
- **New hardware and software design paradigms** together with **new analysis techniques** are required.

COTS Processors

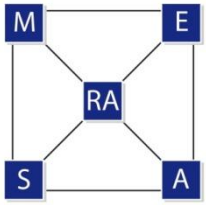
- **COTS (common of-the shelf) processors** contain features that make a WCET analysis hard or even impossible, as e.g.
  - Complex branch prediction (near to impossible)
  - Out-of-order instruction queues (impractical)
  - Instruction caches (hard, but can be done)
  - Data caches (difficult)
  - Two level cache hierarchy (even more difficult)
  - Complex DRAM technologies (impractical)
  - Simultaneous multithreading (SMT), hyperthreading (impossible)
- COTS processors are designed for **high average performance, not for timing predictability**

COTS Multi-Cores

- **COTS multi-core processors** bring in additional handicaps for hard real-time tasks
  - Bus is shared among the cores, bus conflicts possible
  - Shared secondary cache
  - Access to memory must be arbitrated
  - I/O and interrupt handling
- Again, COTS multi-core processors are designed for **high average performance, not for timing predictability**

Solution: Multi-Core Processors

- Our solution based on multi-core systems:
  - Exemplary **parallelisation of industrial applications**,
  - **parallelisation support techniques**,
  - in concert with **WCET technology**, **verification tools**, **system architecture**,
  - and **multi-core embedded processor** technology.
- **parMERASA project** (2011-2014) is application-driven and is based on
- **predecessor project MERASA** (2007-2010), which was hardware-driven.



MERASA Project Achievements

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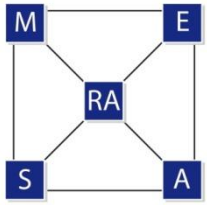
- **Predecessor project: MERASA multi-core architecture**
  - **Timing-predictable** (bus-based) **multi-core** architecture based on **in-order SMT cores**
  - One **hard real-time** task per core in **isolation**
  - Capable of **mixed execution** of hard real-time and non real-time applications
  - System software and tool support (Otawa and RapiTime)

Hard real-time support by full **isolation of tasks** and **bounding of interferences** can be reached. However, MERASA design not scalable over 4-8 cores.



MERASA Project Achievements

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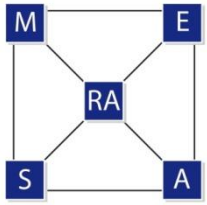
MERASA provided a **Step Towards Time-Predictable Execution of Parallelized HRT Tasks** by

Combination of Software and Hardware Techniques

- Coding guidelines for parallelisation and WCET analysability
- Fully time predictable multi-core processor design
  - isolation as far as possible or
  - bounding timing effects in case of shared resources
  - synchronisation support by hardware
- Time predictable system software and verification tools



MERASA Project Achievements

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- **Applications by Honeywell International**
  - **Parallelized collision avoidance algorithm**
    - runs on simulators and FPGA prototype,
    - analysed with both WCET tools,
    - used in demonstrator of "autonomously flying vehicle simulator".
  - **Parallelized stereo navigation algorithm**
    - is too resource demanding for low-level simulator and FPGA,
    - runs in selected parts on high-level simulator,
    - partly analysed with both WCET tools,
    - Features a parallelism degree of up to 50!
- **Preliminary Pilot Study with BAUER Maschinen GmbH**
    - Parallelization of existing sequential control code
    - Distribution of subtasks over different cores
    - reduction of the RapiTime based WCET of nearly 50% with four cores

Targets

Multi-Core Execution of *parallelised* Hard Real-Time Applications Supporting Analysability

EC FP-7 project started: Oct. 1, 2011, 3 years

3.3 Mio € EC contribution

Project webpage: http://www.parmerasa.eu

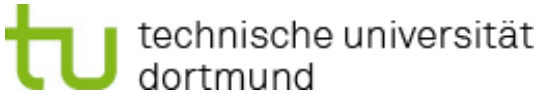
- Find ways to **efficiently parallelise industrial applications** for embedded real-time systems.
- Provide **hard real-time support in system software, WCET analysis and verification tools for multi-cores**.
- Develop techniques for **time predictable multi-cores with 16 to 64 cores** which are commercially feasible.
- Contribute to **Standards** and **Open Source Software**.

Project Partners

- **University of Augsburg** (Project Coordinator) Germany

- **Barcelona Supercomputing Center** Spain

- **Université Paul Sabatier** Toulouse, France



- **Technical University of Dortmund** Germany

- **Rapita Systems Ltd.** York, UK

- **Honeywell international s.r.o.** Brno, Czech Republic

- **BAUER Maschinen GmbH** Schrobenhausen, Germany

- **DENSO AUTOMOTIVE Deutschland GmbH** Eching, Germany

Industrial Advisory Board

- **Airbus,** Toulouse, France, avionic domain
- **European Space Agency ESA**, Noordwijk, The Netherlands, space domain
- **Infineon Technologies UK Ltd**, Bristol, UK, embedded multi-core processor
- **Infineon Technologies AG**, Dept. Industrial & Automotive, Munich, Germany, automotive and AUTOSAR Standardisation Task Force on Safety
- **BMW Group**, Munich, Germany, automotive, AUTOSAR Standardisation Task Force on Safety, and ISO 26262 Standardisation Committee
- **MECEL AB**, Sweden, automotive and ISO 26262 Standardisation Committee
- **Elektrobit Automotive GmbH**, Erlangen, Germany, automotive, in particular AUTOSAR on multi-core systems and AUTOSAR Standardisation

SMART Objectives

Specific, Measurable, Achievable, Realistic, Timely

- O1: Software engineering approach targeting WCET-aware parallelisation techniques and parallel execution patterns
  - Development path leading from sequential legacy programs to parallel programs
  - **Find at least four patterns that are analysable**
- O2: Parallelisation of industrial case studies by applying the software engineering approach and suitable parallel execution patterns.
  - **Achieve at least an eightfold WCET speedup.**
- O3: On target verification tools
  - **WCET analysis with less than 25% pessimism on WCET estimates of parallel programs.**
  - Tools for code coverage, memory analysis, parallel program profiling and visualisation.
- O4: System architecture and system-level SW that supports WCET analysable parallelisation
  - Common micro-kernel basis and application domain specific run-time environments

SMART Objectives

Specific, Measurable, Achievable, Realistic, Timely

- O5: Scalable and timing analysable multi-core processor
  - at least a **16x average speed-up with 64 cores**
  - simulator prototype able to **simulate at least 500,000 instructions per second**.
- O6: Contribute to standards
  - **at least four recommendations to either automotive or avionics standards**.
  - concept for applying the developed parallel execution patterns to AUTOSAR and the IMA standard ARINC 653.
- O7: Contribute to **Open Source software**
  - software developed at the universities, i.e. the static WCET tool OTAWA, the developed system software and the parMERASA simulator, will be made publicly available under an Open Source license at the end of the parMERASA project.

Conclusions

- **Hard real-time demands** in safety critical areas require **timing predictable multi-cores**.
- **MERASA project** showed that **timing predictable multi-core design together with adapted WCET tools and system software** can be achieved
- **parMERASA project** targets **application parallelisation** such that timing predictability can still be guaranteed

MERASA and parMERASA Vision

- **Application companies** in safety critical areas should **demand timing predictable multi-cores**.
  - WCET analysis and verification instead of or additionally to testing.
- **Safety standards and certifications** should be **tightened to demand such processors**.
- **Higher performance demand** may – in future – be satisfied by **multi-cores with more than 16 cores**.

Our Vision

Make **timing predictable** techniques commercially feasible to **increase safety** in **aerospace**, **automation** and **automotive** domains!